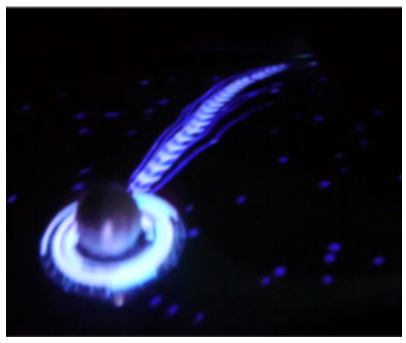
FPGA Implementation of 784fps and 1ms Delay Tracking Using Local-search Based Feature Detection and Sub-pixel Block Matching

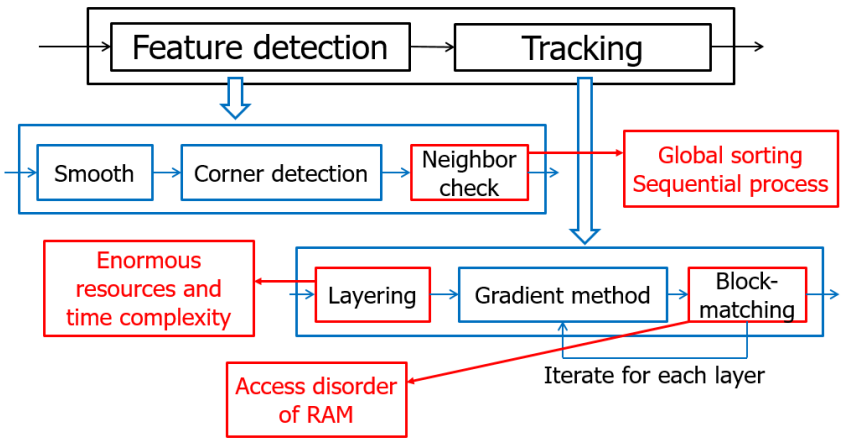
修士課程卒業　呉　宏

Research Background



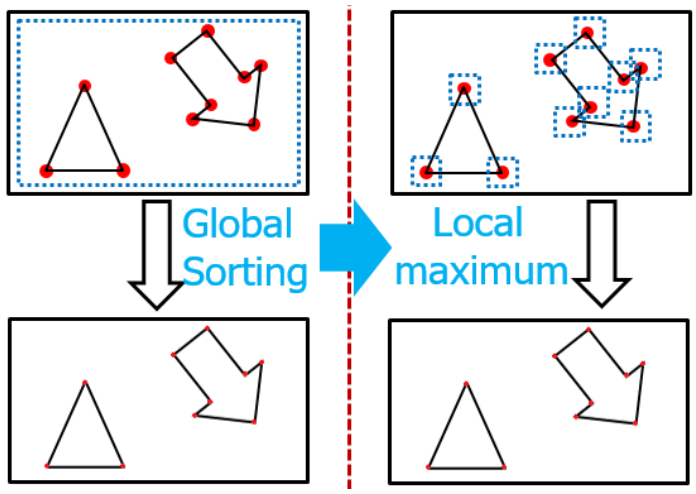

Projection mapping

https://www.youtube.com/watch?v=evwoSfrC9aM (left)
http://channel.panasonic.com/jp/contents/16913/ (right)

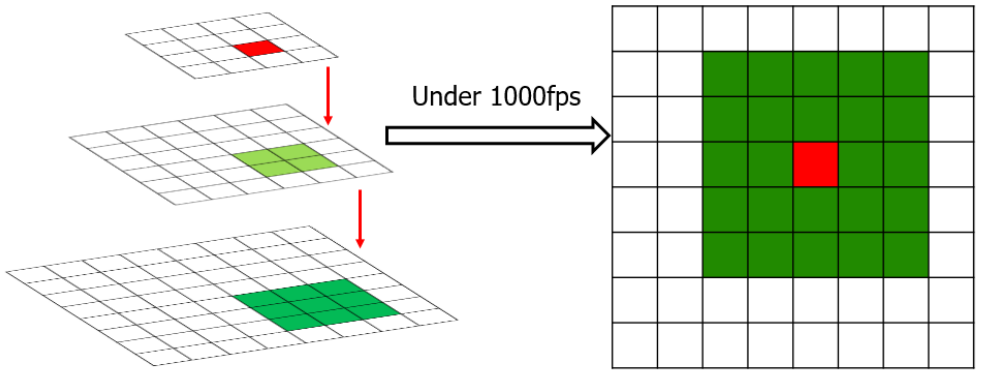


Target: High frame rate and ultra-low delay tracking system using FPGA board.

Proposals

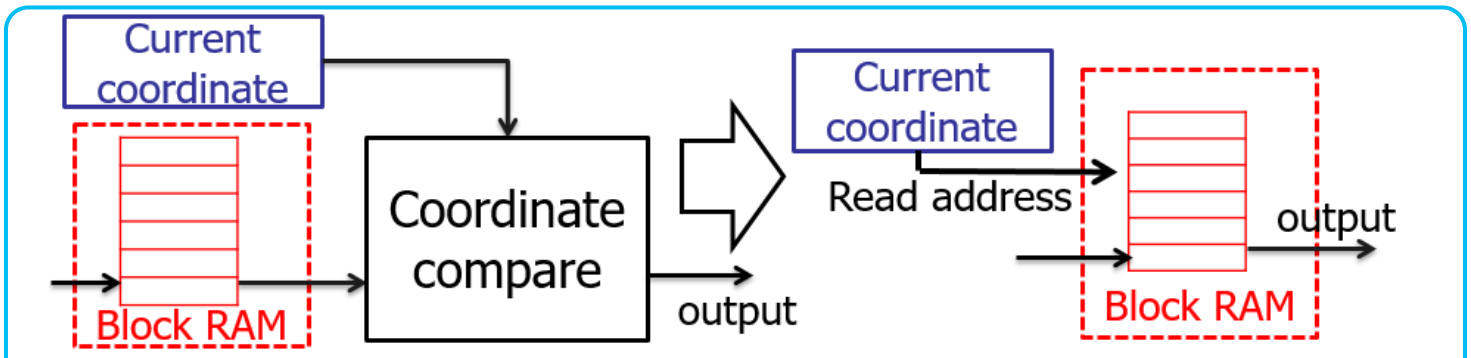


Proposal 1:Local maximum neighboring check



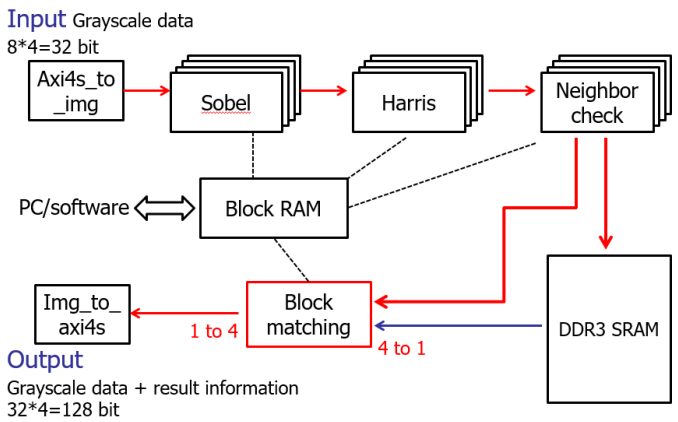
KLT:
Construct pyramid
+float number iterations

Proposal 2:
Search surrounding + sub-pixel
can achieve the same accuracy.



Proposal 3:Coordinate-addressed feature storage

Experiment result:



Comparison with original KLT

	KLT	Proposal
Numbers of slice registers	110192	106800
Numbers of slice LUTs	74185	177172
Numbers of occupied slices	42085	45296
Numbers of DSP48E1s	119	28
Total process time	8.25ms	0.762ms

Conclusion:

Based on the KLT framework I localize the whole algorithm and implement the simplified optical flow tracking algorithm with a quarter sub-pixel precision. The whole system works at 784 fps and within 1ms delay and the video resolution is 640*480, a standard VGA size.

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